Variability study of high current junctionless silicon nanowire transistors

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INTRODUCTION

Silicon nanowires have numerous potential applications, including transistors, memories, photovoltaics, biosensors and qubits [1]. Fabricating a nanowire with characteristics required for a specific application, however, poses some challenges. For example, a major challenge is that as the transistors dimensions are reduced, it is difficult to maintain a low off-current (I_{off}) whilst simultaneously maintaining a high on-current (I_{on}). This can be the result of quantum mechanical tunnelling, short channel effects or statistical variability [2]. A variety of new architectures, including ultra-thin silicon-on-insulator (SOI), double gate, FinFETs, tri-gate, junctionless and gate all-around (GAA) nanowire transistors, have therefore been developed to improve the electrostatic control of the conducting channel. This is essential since a low I_{off} implies low static power dissipation and it will therefore improve power management in the multi-billion transistor circuits employed globally in microprocessors, sensors and memories.

Here we demonstrate a solution by exploiting the quantum effects of a 1-dimensional (1D) Si nanowire transistor (NWT). Whilst 1D devices have been produced in many material systems [3] here we analyse 1D nanowires in a scalable, top-down Si technology. According to the scaling theory of localisation [4], metallic behaviour from high doping levels can only occur in 3D materials but such metallic material cannot be depleted by electrostatic gates.

METHODOLOGY AND DISCUSSION

All simulations of this study, that analyses gated high doped Si NWT, are carried out by a means of the drift-diffusion (DD) module (including density-gradient quantum corrections, DG) [5]. For the purpose of this study, we assume that the DG reproduces accurately the quantum confinement effects, which is a valid approximation for the wire with such a cross-section dimension [6]. Currently work is being undertaken toward calibrating the DG correction to the 2D Schrodinger-3D Poisson solver, used for accurate simulation of quantum confinement effects. Also, the fabrication techniques and electronic properties of similar ungated and larger nanowires have been published elsewhere [6].

Fig. 1 shows experimental results for the drain current as a function of the gate voltage measured for five different drain biases. The nanowire diameter is measured by a transmission electron microscope (TEM), which clearly distinguishes the Si nanowire core from its SiO_2 surroundings as illustrated in Fig. 1 (inner part). The I_{on} to I_{off} ratio is above 10^8. The sub-threshold slope (SS) is 66 mV/dec which is close to the theoretical minimum of 60 mV/dec at room temperature.

Fig. 2 compares the experiment and simulation results demonstrating that a good match between the experimental data and simulation results has been achieved. This good match is accomplished by calibrating the electron mobility. Importantly, a correct calibration of the simulation results to the experimental data has been achieved not only for the low drain voltages but also for the high drain voltages. Small discrepancies, however, in the sub-threshold slope (SS) remain since the 3D TCAD nanowire model is a smooth device without any source of statistical variability and oxide traps.

Fig. 3 presents device simulations of the realistic nanowire with a gate length of 150 nm and a NWT diameter of 8 nm. The same figure reveals a 2D cut through the middle of the device. As expected, the current density increases as the gate voltage is increased. More importantly, it is visible from Fig. 3 that the charge transport is through the middle of the channel which is consistent with the operation mode of junctionless devices. When the gate voltage is below V_T the device is in a depletion mode. In the case when the gate is above V_T, the transistor is in a partial depletion state.

Fig. 4 confirms the electron transport and the current flow through the body of the channel. This figure shows the current density magnitude along the channel for different values of the gate voltage. At the low gate biases the transistor is turned off due to an electrostatic pinch-off. At the high gate biases, well above V_T, the device operates in flat-band conditions and, as a result, the current pathway is through the body of the transistor. As a result, we are confident that our simulation results not only can accurately reproduce the experimental I_D–V_G curves but they also accurately capture the underlying physics in junctionless nanowire devices.

Each plot in Fig. 5 shows 150 devices with four gate lengths of L_G=150, L_G=100, L_G=50 and L_G=25 nm assuming random dopants fluctuation (RDF) as a source of statistical variability (SV). The results reveal that the mean value of the OFF-current for L_G=150 nm and L_G=100 nm is almost the same. Also, both types of devices show very similar distribution and standard deviation of the I_{OFF}. The median of the ON-current decreases with shrinking of the device gate length. More importantly, devices with a 25 nm gate length also have a good I_{ON}/I_{OFF} ratio which makes them useful for practical application such as a transistor.

Fig. 6 and Fig. 7 reveal some of the most important Figures of Merit (FoM) for those 150 devices at each gate length assuming RDF. As expected, there is a strong negative correlation between V_T and I_{OFF} which is consistent for all devices. There is almost no correlation between the other main parameters, such as the I_{OFF} and I_{ON}.

Fig. 8 shows the most extreme cases for transistors with L_G=25 nm and L_G=150 nm. Due to a specific doping configuration, it is possible for a nanowire with L_G=25 nm to have similar I_D-V_G characteristics to the devices with L_G=150 nm that have the worst results. Hence, it is possible to fabricate a device with a 25 nm gate length and for this device to still show excellent I_{ON}/I_{OFF} ratio typical for a transistor. We expect these results to allow us to optimise the NWTs design and to improve the device performance which could be used for low-power applications and metrology.

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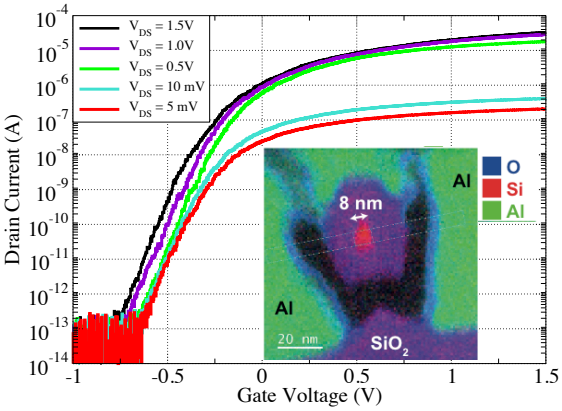

Fig. 1 The experimentally recorded drain current, I_D as a function of gate voltage for the 8 nm Si nanowire for a range of drain currents from 5 mV to 1.5 V at 293 K. The insert is an elemental map of a cross-section.

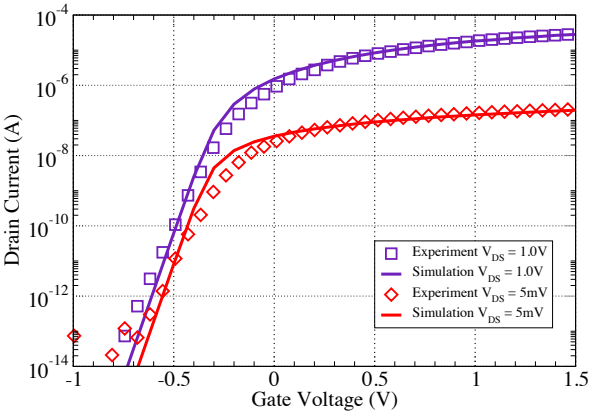

Fig. 2 A comparison between the experimental data (symbols) and the simulations for a drain bias (V_{DS}) of 1.0 V (violet) and 5 mV (red).

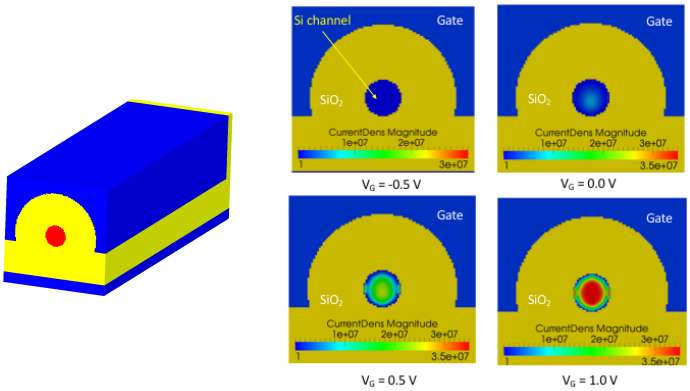

Fig. 3 Left: A 3D view of the nanowire showing the used materials. Right: A cut through the middle of the nanowire showing a cross-section of the device. The current density is shown in the channel region. Red is the Si channel, yellow is SiO_2 and blue is the contact region. The drain bias is V_D = 1.0 V.

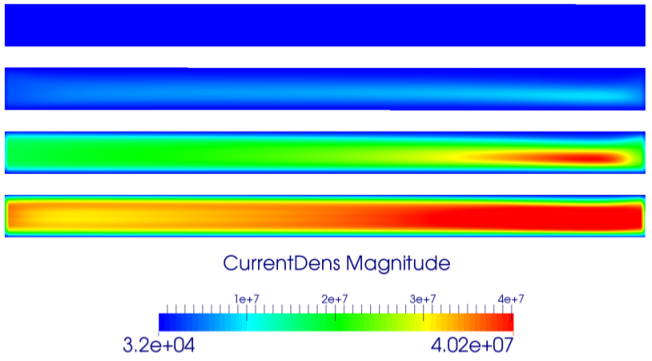

Fig. 4 A 2D profile of current density along the wire. The cut is through the middle of the wire. From top to bottom V_G=-0.5, V_G=0.0, V_G=0.5 V_G=1.0V.

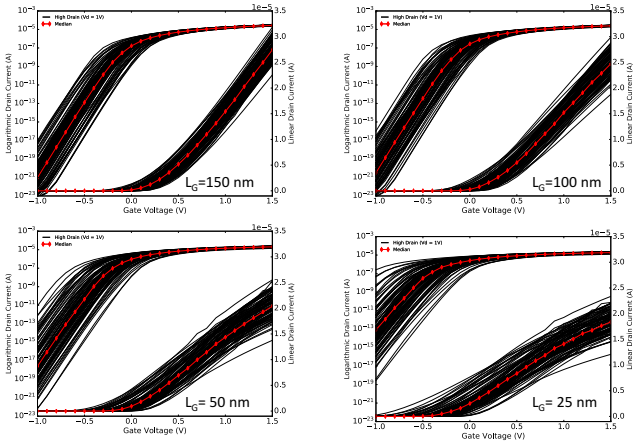

Fig. 5 The drain current vs. gate voltage characteristics of devices with four gate lengths of 150 nm, 100 nm, 50 nm and 25 nm. In each case 150 devices with various positions of the dopants are considered as a source of variability.

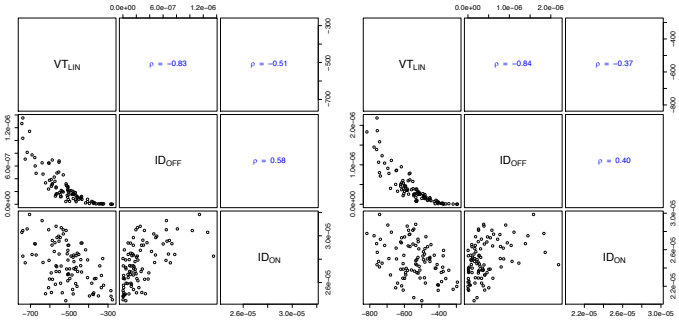

Fig. 6 Correlation between Figures of Merit (FoM) obtained from the physical simulations for 150 devices with L_G=150 nm and L_G=100 nm.

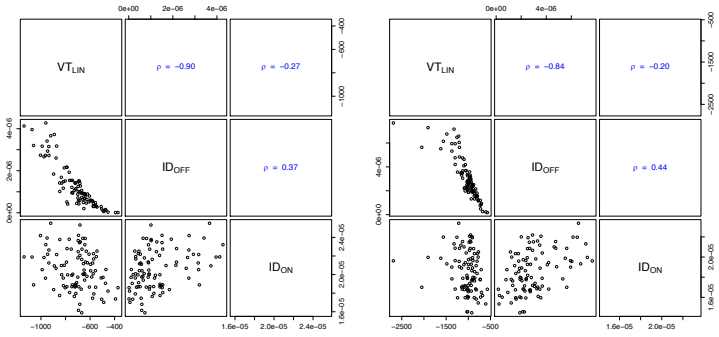

Fig. 7 Correlation between Figures of Merit (FoM) obtained from the physical simulations for 150 devices with L_G=50 nm and L_G=25 nm.

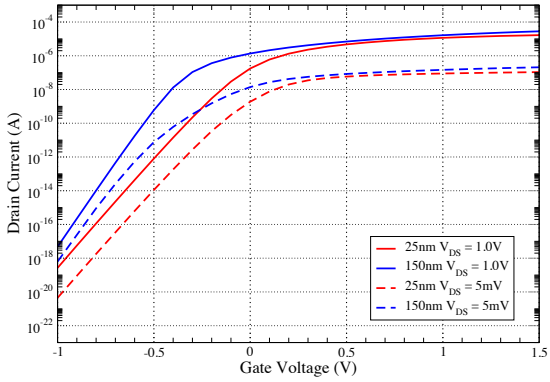

Fig. 8 Comparison between the drain current and the gate voltage characteristics for the most extreme case from all 150 devices with L_G=25 nm and L_G=150 nm in the case of a high and low drain bias.